



(12) **United States Patent**  
**Lee et al.**

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(54) **METHOD TO MANAGE CURRENT DURING  
CLOCK FREQUENCY CHANGES**

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CPC . **G06F 1/08** (2013.01); **G06F 1/324** (2013.01)

(58) **Field of Classification Search**  
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See application file for complete search history.

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(57) **ABSTRACT**

A system for managing a change in a frequency of a clock signal, including a clock generator configured to output the clock signal, a clock divider coupled to the output of the clock generator, a processor configured to select the frequency of the clock signal, and a clock management circuit. The clock management circuit may be configured to set the clock generator to adjust the clock signal to the selected frequency. The clock management circuit may be further configured to adjust a divisor value of the clock divider in a plurality of steps in response to a determination the clock signal stabilized at the selected frequency. A new divisor value may be selected during each step in the plurality of steps and each step may occur after a given time period.

**20 Claims, 5 Drawing Sheets**

